KANDULA SRINIVASA REDDY MEMORIAL COLLEGE OF ENGINEERING
(AUTONOMOUS)

KADAPA-516003. AP

(Approved by AICTE, Affiliated to JNTU A, Ananthapuramu, Accredited by NAAC)

(An ISO 9001-2008 Certified Institution)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Certification Course

On

"Advanced VLSI Concepts"

Resource Persons : Sri.R.V.Srihari, Assoc.Professor Dept. of ECE, KSRMCE

Sri.N.Nagendra prasad, Assistant professor, Dept. of ECE, KSRMCE

Course Coordinators: Smt.M.Tulasi, AssistantProfessor Dept. of ECE, KSRMCE

Smt.K.Lakshmi prasanna, Assistant professor, Dept. of ECE, KSRMCE

Duration : 04/03/2019 to 21/03/2019

K.S.R.M. COLLEGE OF ENGINEERING

(UGC-AUTONOMOUS)

Kadapa, Andhra Pradesh, India– 516 003

Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

An ISO 14001:2004 & 9001: 2015 Certified Institution

Lr./KSRMCE/ECE/2018-19/

Date:28/02/2019

To
The Principal,
KSRMCE,
Kadapa.

Respected Sir,

Sub: Permission to Conduct Certification Course on "**Advanced VLSI Concepts**" **04/03/2019 to 21/03/2019**–Req- Reg.

The Department of Electronics and communication engineering is planning to offer a Certification Course on "Advanced VLSI Concepts" to B. Tech. students. The course will be conducted from **04/03/2019 to 21/03/2019**. In this regard, I kindly request you to grant permission to conduct a Certification Course.

Thanking you sir,

Yours faithfully

(Smt.K.Lakshmi prasanna, Asst.Professor in ECED)

Forwarded to the Principal sir

V. S. S. Murty
PRINCIPAL
K.S.R.M. COLLEGE OF ENGINEERING
KADAPA-516005, (A.P.)

K.S.R.M. COLLEGE OF ENGINEERING

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Kadapa, Andhra Pradesh, India– 516 003

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Cr./KSRMCE/ECE/2018-19/

Date: 01/03/2019

Circular

The Department of Electronics and Communication Engineering is offering a Certification Course on "Advanced VLSI Concepts" from **04/03/2019 to 21/03/2019** to B.Tech students. In this regard, interested students are requested to register their names for the Certification Course with Course Coordinator.

For further information contact the Course Coordinator.

Course Coordinator: Smt.K.Lakshmi Prasanna, Asst.professor, Dept. of ECE.-KSRMCE.

HoD

Dept. of ECE

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

Cc to:

IQAC-KSRMCE

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Date:

DEPARTMENT OF ECE

REGISTRATION FORM

Certification Course

On

"Advanced VLSI Concepts" From 04/03/2019 to 21/03/2019

S.No	Full Name	Roll Number	Branch	Semester	Signature

Coordinator(s) HoD

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DEPARTMENT OF ECE

REGISTRATION FORM

Certification Course
On
"Advanced VLSI Concepts" From 04/03/2019 to 21/03/2019

S.No	Full Name	Roll Number	Branch	Semester	Signature
1	Agnikondu Ramkumar	169Y1A0401	ECE	VI SEM	A.Ramkumar
2	Akkisetty Chandana Priya	169Y1A0402	ECE	VI SEM	A.chandana
3	Akula Gurusai Krishna	169Y1A0403	ECE	VI SEM	A.Gurusai
4	Annapureddy Kalyani	169Y1A0404	ECE	VI SEM	A.kalyani
5	Arava Sai Sushmitha	169Y1A0405	ECE	VI SEM	A.sushmitha
6	Arcot Mohammad Arshad	169Y1A0406	ECE	VI SEM	A.Arshad
7	Athikari Guru Prakash	169Y1A0407	ECE	VI SEM	A.Guruprakash
8	Banreddy Sivateja Reddy	169Y1A0409	ECE	VI SEM	B.Sivateja
9	Chowdam Sudarshan	169Y1A0421	ECE	VI SEM	C.sudarshan.
10	Gaddam Rachana	169Y1A0429	ECE	VI SEM	G.Rachana
11	Gajjala Deepthi	169Y1A0430	ECE	VI SEM	G.Deepthi
12	Galla Manisha	169Y1A0431	ECE	VI SEM	G.Anil Kumar
13	Gondipalle Anil Kumar	169Y1A0432	ECE	VI SEM	G.
14	Gontimukkala Venkata Kalyan	169Y1A0433	ECE	VI SEM	GV.Kalyan
15	Gosula Sreesai	169Y1A0434	ECE	VI SEM	G.Sreesai
16	Goturu Anusha	169Y1A0435	ECE	VI SEM	G.Anusha
17	Gundarapu Kishore	169Y1A0436	ECE	VI SEM	G.Kishore
18	Gundluri Vinitha	169Y1A0437	ECE	VI SEM	G.Vinitha
19	Nandipati Amareswara Reddy	169Y1A0468	ECE	VI SEM	N.A.Reddy
20	Nandivada Harika	169Y1A0469	ECE	VI SEM	N.Harika
21	Neelam Saikrishna	169Y1A0470	ECE	VI SEM	N.Saikrishna
22	Obulareddy Chaitanya Reddy	169Y1A0471	ECE	VI SEM	O.chaithanya
23	Onteddu Padmaja	169Y1A0472	ECE	VI SEM	O.padmaja
24	Pamireddy Sreenivasulu Reddy	169Y1A0473	ECE	VI SEM	P.Sreenu

25	Panchi Sadathullah	169Y1A0474	ECE	VI SEM	P. Sadathulla
26	Pileti Venkata Krishna	169Y1A0481	ECE	VI SEM	
27	Sareddy Kshema	169Y1A0490	ECE	VI SEM	Sareddy
28	Shaik Afra Arsheen	169Y1A0491	ECE	VI SEM	S. Afra Arsheen
29	Shaik Mahaboob Asif	169Y1A0492	ECE	VI SEM	S. Mahaboob
30	Singam Reddy Madhusudan Reddy	169Y1A0493	ECE	VI SEM	SRMR

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
KADAPA - 516 003

Syllabus of Certification Course

Course name : Advanced VLSI Concepts

Course objectives:

1. To provide rigorous foundation in MOS and CMOS digital circuits
2. To train the students in transistor budgets, clock speeds and the growing challenges of power consumption and productivity.

Course outcomes:

After studying this course, students will be able to:

1. Analyze the CMOS circuit and its use
2. Estimate the circuit Performance
3. Design Various CMOS logic design circuits
4. Understand the design of a systems and its methods
5. Design various subsystems

UNIT-I

INTRODUCTION TO CMOS CIRCUITS

MOS Transistors, MOS Transistors switches, CMOS logic circuit and System representations, MOS Transistor theory – Introduction MOS device design equation, the complementary CMOS inverter – DC characteristics, Static Load MOS inverters, The differential inverter, The transmission gate, The Tri state inverter, Bipolar Devices.

UNIT-II

CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION

Introduction, Resistance estimation, Capacitance estimation, Inductance estimation, Switching characteristics of CMOS gate Transistor, Sizing, Power Dissipation, Sizing Routing conductors, Charge sharing, Design Margining, Reliability.

UNIT-III

CMOS CIRCUIT AND LOGIC DESIGN

CMOs Logic Gate design, Basic Physical Design of simple gate, CMOS Logic structures clocking strategies, i/o Structures, Low Power Design.

UNIT-IV

SYSTEMS DESIGN AND DESIGN METHOD

Design Strategies CMOS chip Design options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, and Data Sheets.

Unit-V

CMOS Testing

Manufacturing Test Principles, Design Strategies for Test, Chip level Test Techniques, System Level Test Techniques, and Layout Design for Improved Testability.

Text Books:

1. N.H.E.Weste&D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th

Edition, Pearson, 2011.

2. J.Rabey& B. Nikolic, "Digital Integrated circuits", 2 ndEdition,Pearson, 2003.1

Reference Books:

1. P.E.Allen&D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University

Press, 2011. 2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd

Edition, Wiley, 2010

Professor & H.O.D.
Department of E.C.E.
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SCHEDULE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Certification Course

On

"Advanced VLSI Concepts" From 04-03-2019 to 21-03-2019

Date	Timing	Resource Person	Topic to be covered
04/03/2019	2 PM to4PM	Sri.R.V.Srihari Sri.N.Nagendraprasad	**UNIT I** INTRODUCTION TO CMOS CIRCUITS MOS Transistors
04/03/2019	4PM to 5PM	Sri.R.V.Srihari	MOS Transistors switches
05/03/2019	2 PM to4PM	Sri.N.Nagendraprasad	CMOS logic circuit and System representations
05/03/2019	4PM to 5PM	Sri.R.V.Srihari	MOS Transistor theory – Introduction MOS device design equation,
06/03/2019	2 PM to4PM	Sri.N.Nagendraprasad	The complementary CMOS inverter – DC characteristics
06/03/2019	4PM to 5PM	Sri.R.V.Srihari	Static Load MOS inverters
07/03/2019	2PM to 4PM	Sri.N.Nagendraprasad	The differential inverter
07/03/2019	4PM to 5PM	Sri.R.V.Srihari	The transmission gate
08/03/2019	2PM to 4PM	Sri.N.Nagendraprasad	The Tri state inverter, Bipolar Devices..
08/03/2019	4PM to 5PM	Sri.R.V.Srihari	**UNIT-II:** CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION Introduction, Resistance estimation
11/03/2019	2PM to 4PM	Sri.N.Nagendraprasad	Capacitance estimation, Inductance estimation
11/03/2019	4PM to 5PM	Sri.R.V.Srihari	Switching characteristics of CMOS gate.
12/03/2019	3PM to 4PM	Sri.N.Nagendraprasad	Transistor Sizing, Power

			Dissipation
12/03/2019	4PM to 5PM	Sri.R.V.Srihari	Sizing Routing conductors
13/03/2019	2PM to 4PM	Sri.N.Nagendraprasad	Charge sharing
13/03/2019	4PM to 5PM	Sri.R.V.Srihari	Design Margining, Reliability.
14/03/2019	2PM to 4PM	Sri.N.Nagendraprasad	**UNIT III** CMOS CIRCUIT AND LOGIC DESIGN : CMOs Logic Gate design
14/03 /2019	4PM to 5PM	Sri.R.V.Srihari	Basic Physical Design of simple gate
15/03/2019	3PM to 4PM	Sri.N.Nagendraprasad	CMOS Logic structures
15/03/2019	4PM to 5PM	Sri.R.V.Srihari	clocking strategies.
16/03/2019	3PM to 4PM	Sri.N.Nagendraprasad	I/OStructures, Low Power Design
16/03/2019	4PM to 5PM	Sri.R.V.Srihari	**UNIT-IV** SYSTEMS DESIGN AND DESIGN METHOD Design Strategies CMOS chip Design Options
17/03/2019	2PM to 4PM	Sri.N.Nagendraprasad	Design Methods, Design Capture Tools
17/03/2019	4PM to 5PM	Sri.R.V.Srihari	Design Verification Tools
18/03/2019	3PM to 4PM	Sri.N.Nagendraprasad	Design Economics, and Data Sheets
18/03/2019	4PM to 5PM	Sri.R.V.Srihari	CMOS Testing – Manufacturing Test Principles
19/03/2019	3PM to 4PM	Sri.N.Nagendraprasad	Design Strategies for Test
19/03/2019	4PM to 5PM	Sri.R.V.Srihari	Chip level Test Techniques,
21/03/2019	3PM to 4PM	Sri.N.Nagendraprasad	System Level Test Techniques
21/03/2019	4PM to 5PM	Sri.R.V.Srihari	Layout Design for Improved Testability

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.
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DEPARTMENT OF ECE

Attendance Sheet of Certification Course on "Advanced VLSI Concepts"

From 04/03/2019 to 21/03/2019

S. No.	Roll No.	Name	04/03/2019	05/03/2019	06/03/2019	07/03/2019	08/03/2019	11/03/2019	12/03/2019	13/03/2019	14/03/2019	15/03/2019	16/03/2019	18/03/2019	19/03/2019	20/03/2019	21/03/2019
1	169Y1A0401	Agnikondu Ramkumar	P	A	P	P	P	P	P	P	P	P	P	P	A	P	P
2	169Y1A0402	Akkisetty Chandana Priya (W)	P	P	P	P	P	A	P	P	P	P	P	P	P	P	P
3	169Y1A0403	Akula Gurusai Krishna	P	P	A	P	P	P	P	P	P	P	P	P	P	P	A
4	169Y1A0404	Annapureddy Kalyani	P	P	P	P	P	P	A	P	P	P	P	P	P	P	P
5	169Y1A0405	Arava Sai Sushmitha	P	P	A	P	P	P	P	P	P	P	P	P	A	P	A
6	169Y1A0406	Arcot Mohammad Arshad	P	P	P	P	P	P	P	A	P	P	P	P	P	P	P
7	169Y1A0407	Athikari Guru Prakash	P	P	P	P	P	P	P	P	P	A	P	P	P	P	P
8	169Y1A0409	Banreddy Sivateja Reddy	A	P	P	P	P	P	P	P	P	P	P	P	P	P	P

9	169Y1A0421	Chowdam Sudarshan	P	P	A	P	P	P	P	P	A	P	P	P	P	P	P	A
10	169Y1A0429	Gaddam Rachana (W)	P	P	P	P	P	P	P	A	P	P	P	P	P	P	P	P
11	169Y1A0430	Gajjala Deepthi (W)	P	P	P	P	A	P	P	P	P	P	P	P	P	P	P	P
12	169Y1A0431	Galla Manisha (W)	P	A	P	P	P	P	P	P	A	P	P	P	P	P	P	A
13	169Y1A0432	Gondipalle Anil Kumar	P	P	P	P	P	P	P	P	P	A	P	P	A	P	P	P
14	169Y1A0433	Gontimukkala Venkata Kalyan	P	P	P	P	P	P	P	P	P	P	P	A	P	A	P	P
15	169Y1A0434	Gosula Sreesai (W)	P	P	P	P	P	P	A	P	P	P	A	P	P	P	P	P
16	169Y1A0435	Goturu Anusha (W)	P	P	A	P	P	P	A	P	P	P	P	P	P	A	P	P
17	169Y1A0436	Gundarapu Kishore	A	P	P	P	P	P	P	P	P	P	P	P	P	A	P	P
18	169Y1A0437	Gundluri Vinitha (W)	P	P	P	P	A	A	P	P	P	P	P	P	P	P	P	P
19	169Y1A0468	Nandipati Amareswara Reddy	P	P	P	P	P	P	P	A	P	P	A	P	P	P	P	P
20	169Y1A0469	Nandivada Harika (W)	P	P	P	P	A	P	P	P	P	P	P	P	P	P	P	P
21	169Y1A0470	Neelam Saikrishna	A	P	P	P	P	P	P	P	P	P	P	P	P	P	A	A
22	169Y1A0471	Obulareddy Chaitanya Reddy	A	P	P	P	A	P	P	P	P	P	P	P	P	P	A	P
23	169Y1A0472	Onteddu Padmaja (W)	P	P	P	P	P	P	A	P	P	P	P	P	P	A	P	A
24	169Y1A0473	Pamireddy Sreenivasulu Reddy	P	P	P	P	P	A	P	P	P	P	P	A	P	P	P	P
25	169Y1A0474	Panchi Sadathullah	P	P	P	P	P	A	P	P	P	P	P	P	P	P	P	P
26	169Y1A0481	Pileti Venkata Krishna	P	A	P	P	P	P	P	P	P	P	P	P	P	P	P	A
27	169Y1A0490	Sareddy Kshema (W)	P	P	A	P	P	P	P	A	P	P	P	A	P	P	A	
28	169Y1A0491	Shaik Afra Arsheen (W)	A	A	P	P	P	P	P	P	P	P	P	A	P	P	P	P

29	169Y1A0492	Shaik Mahaboob Asif	P	A	P	P	P	P	P	P	A	P	P	P	P	A	P
30	169Y1A0493	Singam Reddy Madhusudan Reddy	P	A	P	P	P	P	P	P	P	A	P	P	A	P	P

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
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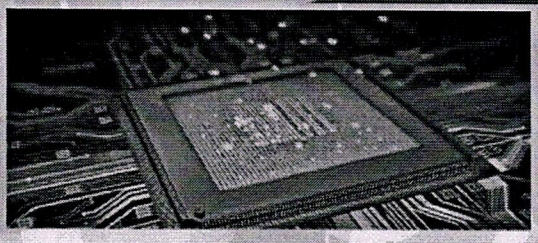
Certification Course
on

Advanced VLSI Concepts



Date:
04-03-2019
21-03-2019

Resource Persons

Sri. N. Nagendra Prasad
Asst.Professor, Dept. Of ECE

Sri. R. V. Srihari
Assoc.Professor, Dept. Of ECE

Venue
DSP Lab

Coordinators

Smt. K. Lakshmi Prasanna
Asst.Professor, Dept. Of ECE

Smt. M. Tulasi
Asst.Professor, Dept. Of ECE

Dr. G. HEMALATHA (Professor & Head) | *Dr. V.S.S. Murthy* (Principal) | *Prof. A. MOHAN* (Director) | *Sri K. Sivananda Reddy* (Correspondent,Secretary,Treasurer) | *Sri K. Madan Mohan Reddy* (Vice - Chairman) | *Sri S. Sankar Reddy* (Chairman)

K.S.R.M. COLLEGE OF ENGINEERING

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Report of

Certification Course

On

"Advanced VLSI Concepts"

From 04th Mar 2019 to 21st Mar 2019

Target Group	:	**B.Tech Students**
Details of Participants	:	**30 Students**
Resource persons	:	**Sri.R.V.Sri hari,Assoc.Professor,Dept. of ECE**
		Sri.N.Nagendra prasad,Asst.Professor,Dept. of ECE
Coordinators	:	**Smt.K.Lakshmi Prasanna, Asst. Professor, Dept. of ECE**
		Smt.M.Tulasi, Asst. Professor, Dept. of ECE
Organizing Department	:	**Department of Electronics and Communication Engineering**
Venue	:	**Dsp lab**

Description:

Certification Course on "Advanced VLSI Concepts" was organized by Dept. of ECE from 04-03-2019 to 21-03-2019 . Sri.R.V.Sreehari and Sri N.NagendraPrasad acted as Course instructors. Recent advances in CMOS circuit design, Circuit characterization and performance estimation, Conventional VLSI design flow and its difficulties in dealing with deep submicron CMOS design, Design issues in modern VLSI designs was explained.

Photos

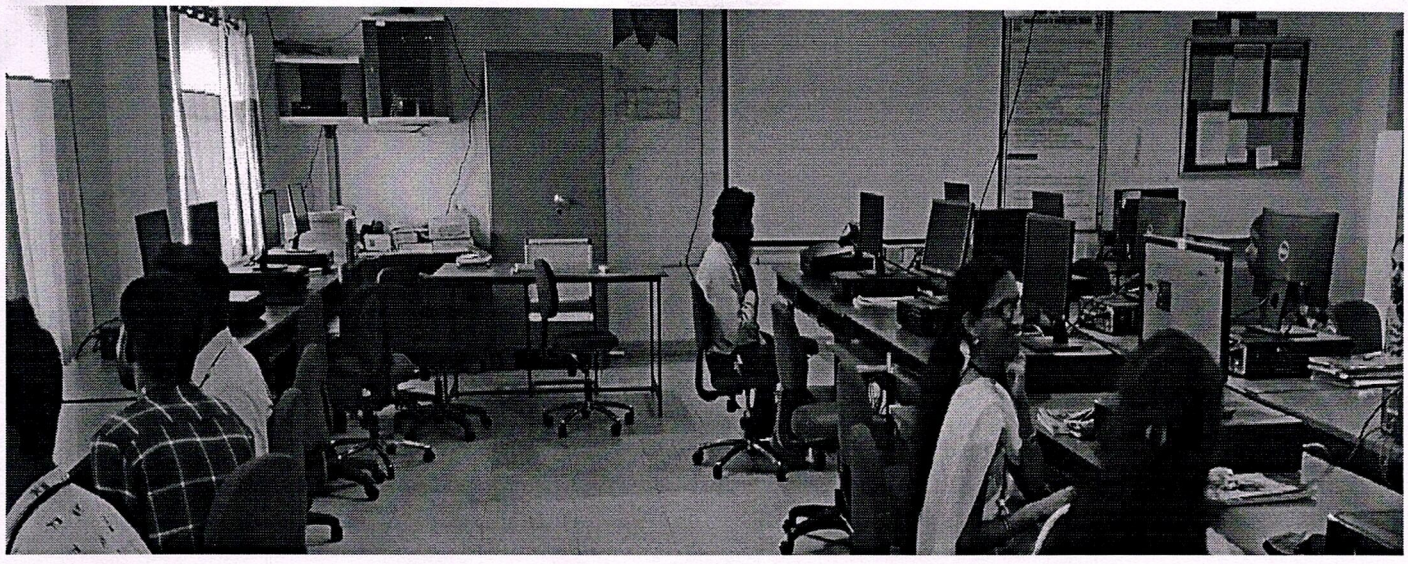

Fig 1: Resource person deliver the lecture

Fig 2: Students listening the lecture

Coordinator(s)

HoD

Professor & H.O.D.
Department of E.C.E.
K.S.R.M. College of Engineering
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Kadapa, Andhra Pradesh, India- 516003.

CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. G. Sreesai *with roll no* 16941A0435 *has completed the Certification Course on "Advanced VLSI Concepts" from 04/03/2019 to 21/03/2019 organized by Department of Electronics and communication engineering.*

Coordinator HoD,ECE Principal

KSRM COLLEGE OF ENGINEERING

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CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. B. Sivateja Reddy *with roll no* 16941A0409 *has completed the Certification Course on "Advanced VLSI Concepts" from 04/03/2019 to 21/03/2019 organized by Department of Electronics and communication engineering.*

Coordinator

HoD,ECE

V. S. S. Murthy
Principal

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CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. A. Guru prakash *with roll no* 15941A0407 *has completed the Certification Course on "Advanced VLSI Concepts" from 04/03/2019 to 21/03/2019 organized by Department of Electronics and communication engineering.*

Coordinator

HoD,ECE

Principal

K.S.R.M. COLLEGE OF ENGINEERING

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Kadapa, Andhra Pradesh, India– 516 003

FEEDBACK FORM

Certification Course on "Advanced VLSI Concepts", from 04-03-2019 to 21-03-2019

Organized

by

Department of Electronics & Communication Engineering

NAME:

Roll No:

S.No	Feedback Item	Excellent	Very Good	Good	Average	Below Average
1	Organization of certificate course and session planning by the instructor.					
2	Clarity in content delivery.					
3	Content is relevant and useful					
4	Adequate opportunity to interact with trainer					
5	Judicious mix of concepts. Principles and practices.					
6	Assignments and tasks are interesting and challenging.					
7	Overall rating					

Any suggestions for improvement.

Signature

K.S.R.M. COLLEGE OF ENGINEERING

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Certification Course On "Advanced VLSI Concepts"

04/03/2019 to 21/03/2019

Feedback responses

S.No.	Roll No	Year & Semester	Branch	Is the course content met your expectation	Is the lecture sequence well planned	The contents of the course is explained with examples	Is the level of course high	Is the course exposed you to the new knowledge and practices	Is the lecturer clear and easy to understand	Rate the value of course in increasing your skills	Any issues
1	169Y1A0401	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	3	5	Nothing
2	169Y1A0402	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	4	very good
3	169Y1A0403	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
4	169Y1A0404	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	very good
5	169Y1A0405	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	5	Nothing
6	169Y1A0406	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	3	Good
7	169Y1A0407	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Good
8	169Y1A0409	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Nothing
9	169Y1A0421	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Nothing

10	169Y1A0429	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	3	Very Good
11	169Y1A0430	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	Good
12	169Y1A0431	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	4	Good
13	169Y1A0432	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	5	Nothing
14	169Y1A0433	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	very good
15	169Y1A0434	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	Nothing
16	169Y1A0435	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	very good
17	169Y1A0436	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	No
18	169Y1A0437	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	3	4	Nothing
19	169Y1A0468	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
20	169Y1A0469	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	3	3	Good
21	169Y1A0470	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good
22	169Y1A0471	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	5	Nothing
23	169Y1A0472	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	Good
24	169Y1A0473	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	4	Good
25	169Y1A0474	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	Good
26	169Y1A0481	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	5	Nothing
27	169Y1A0490	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	No
28	169Y1A0491	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	No
29	169Y1A0492	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	4	3	No

30	169Y1A0493	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	No
31	169Y1A0401	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	4	nothing
32	169Y1A0402	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	5	3	Nothing
33	169Y1A0403	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	4	No
34	169Y1A0404	B.Tech VI sem	ECE	Yes	Yes	agree	Agree	Strongly agree	4	5	Nothing
35	169Y1A0405	B.Tech VI sem	ECE	Yes	Yes	Strongly agree	Agree	Strongly agree	5	5	Good

Coordinator

HoD

Professor & H.O.D.
Department of E.C.E.
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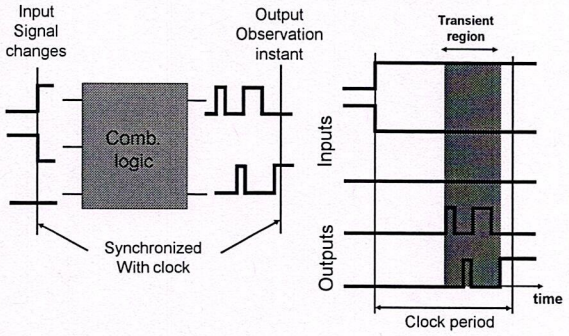
Digital Circuit Timing



Timing Analysis and Optimization

- Timing analysis
  - Dynamic analysis: Simulation.
  - Static timing analysis (STA): Vector-less topological analysis of circuit.
- Timing optimization
  - Performance
  - Clock design
- Other forms of design optimization
  - Chip area
  - Testability
  - Power

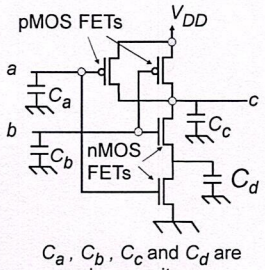
Circuit Delays

- Switching or inertial delay is the interval between input change and output change of a gate:
  - Depends on input capacitance, device (transistor) characteristics and output capacitance of gate.
  - Also depends on input rise or fall times and states of other inputs (second-order effects).
  - Approximation: fixed rise and fall delays (or min-max delay range, or single fixed delay) for gate output.
- Propagation or interconnect delay is the time a transition takes to travel between gates:
  - Depends on transmission line effects (distributed *R*, *L*, *C* parameters, length and loading) of routing paths.
  - Approximation: modeled as lumped delays for gate inputs.

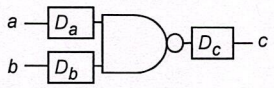
Spice

- Circuit/device level analysis
  - Circuit modeled as network of transistors, capacitors, resistors and voltage/current sources.
  - Node current equations using Kirchhoff's current law.
- Analysis is accurate but expensive
  - Used to characterize parts of a larger circuit.
- Original references:
  - L. W. Nagel and D. O. Pederson, "SPICE – Simulation Program With Integrated Circuit Emphasis," Memo ERL-M382, EECS Dept., University of California, Berkeley, Apr. 1973.
  - L. W. Nagel, *SPICE 2, A Computer program to Simulate Semiconductor Circuits*, PhD Dissertation, University of California, Berkeley, May 1975.

Logic Model of MOS Circuit



C_a, C_b, C_c and C_d are node capacitances



D_a and D_b are interconnect or propagation delays

D_c is inertial delay of gate

Spice Characterization

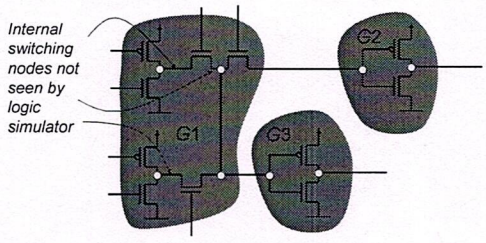
Input data pattern	Delay (ps)	Dynamic energy (pJ)
$a = b = 0 \rightarrow 1$	69	1.55
$a = 1, b = 0 \rightarrow 1$	62	1.67
$a = 0 \rightarrow 1, b = 1$	50	1.72
$a = b = 1 \rightarrow 0$	35	1.82
$a = 1, b = 1 \rightarrow 0$	76	1.39
$a = 1 \rightarrow 0, b = 1$	57	1.94

Spice Characterization (Cont.)

Input data pattern	Static power (pW)
$a = b = 0$	5.05
$a = 0, b = 1$	13.1
$a = 1, b = 0$	5.10
$a = b = 1$	28.5

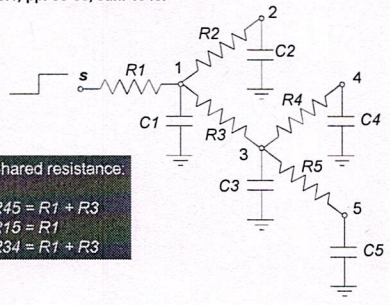
Complex Gates: Switch-Level Partitions

- Circuit partitioned into *channel-connected components* for Spice characterization.
- Reference: R. E. Bryant, "A Switch-Level Model and Simulator for MOS Digital Systems," *IEEE Trans. Computers*, vol. C-33, no. 2, pp. 160-177, Feb. 1984.



Interconnect Delay: Elmore Delay Model

- W. Elmore, "The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers," *J. Appl. Phys.*, vol. 19, no.1, pp. 55-63, Jan. 1948.



Shared resistance:

R45 = R1 + R3
R15 = R1
R34 = R1 + R3

Elmore Delay Formula

Delay at node $k = 0.69 \sum_{j=1}^{N} Cj \times Rjk$

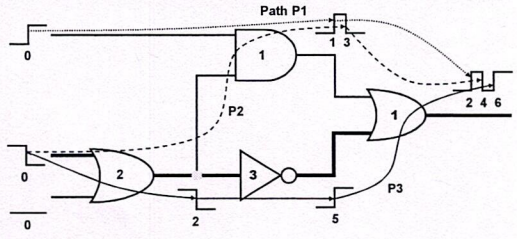
where N = number of capacitive nodes in the network

Example:

Delay at node 5 = 0.69[*R1 C1 + R1 C2 + (R1+R3)C3 + (R1+R3)C4 (R1+R3+R5)C5*]

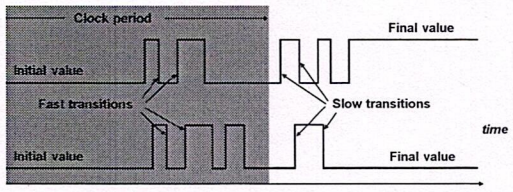
Event Propagation Delays

Single lumped inertial delay modeled for each gate
PI transitions assumed to occur without time skew



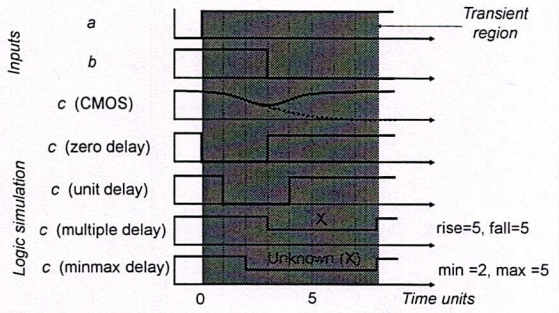
Circuit Outputs

- Each path can potentially produce one signal transition at the output.
- The location of an output transition in time is determined by the delay of the path.



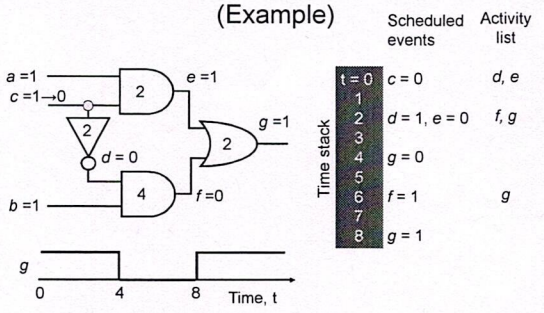
Delay and Discrete-Event Simulation

(NAND gate)

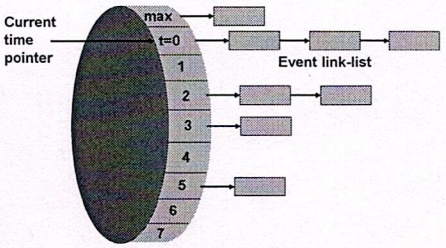


Event-Driven Simulation

(Example)



Time Wheel (Circular Stack)

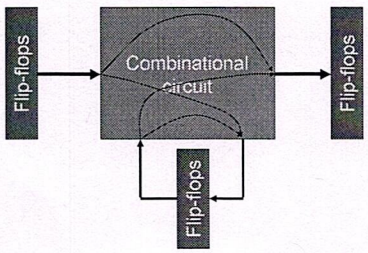


Timing Design and Delay Test

- Timing simulation:
  - Critical paths are identified by static (vector-less) timing analysis tools like *Primetime* (Synopsys).
  - Timing or circuit-level simulation using designer-generated functional vectors verifies the design.
- Layout optimization: Critical path data are used in placement and routing. Delay parameter extraction, timing simulation and layout are repeated for iterative improvement.
- Testing: Some form of at-speed test is necessary. Critical paths and all gate transition delays are tested.

Static Timing Analysis (STA)

- Finds maximum and minimum delays between all clocked flip-flops.



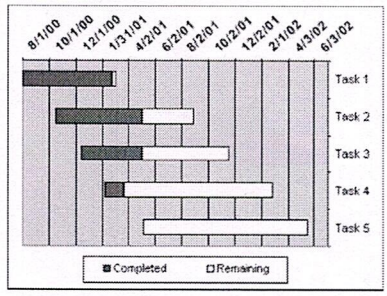
Early References

- T. I. Kirkpatrick and N. R. Clark, "PERT as an Aid to Logic Design," *IBM J. Res. Dev.*, vol. 10, no. 2, pp. 135-141, March 1966.
- R. B. Hitchcock, Sr., "Timing Verification and the Timing Analysis Program," *Proc. 19th Design Automation Conf.*, 1982, pp. 594-604.
- V. D. Agrawal, "Synchronous Path Analysis in MOS Circuit Simulator," *Proc. 19th Design Automation Conf.*, 1982, pp. 629-635.

Basic Ideas

- Adopted from project management
  - Frederick W. Taylor (1856-1915)
  - Henry Gantt (1861-1919)
- PERT – Program Evaluation and Review Technique
- CPM – Critical Path Method

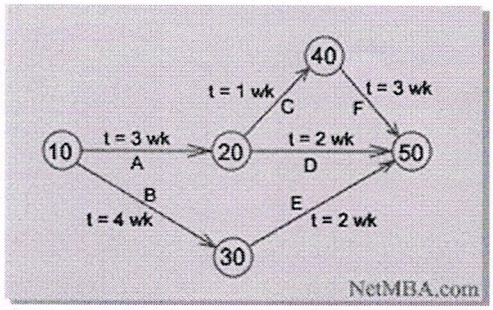
A Gantt Chart in Microsoft Excel



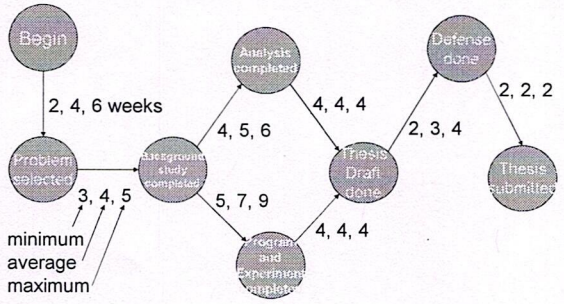
Using a Gantt Chart

- Track progress of subtasks and project.
- Assess resource needs as a function of time.

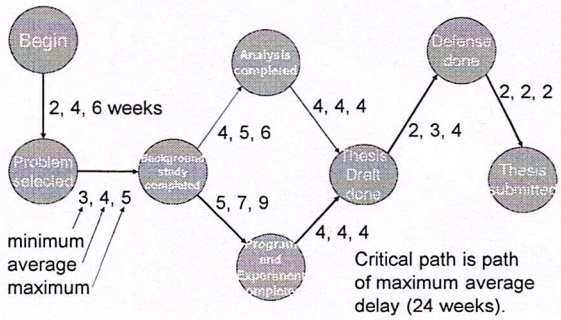
Pert Chart



Example: Thesis Research



Critical Path



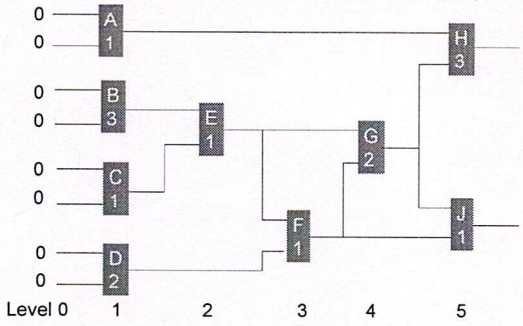
Critical path is path of maximum average delay (24 weeks).

A Basic Timing Analysis Algorithm

- Combinational logic.
- Circuit represented as an acyclic directed graph (DAG).
- Gates characterized by delays.

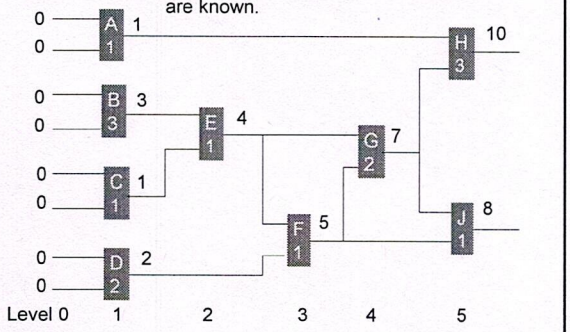
Example

Levelize graph. Initialized arrival times at primary inputs.



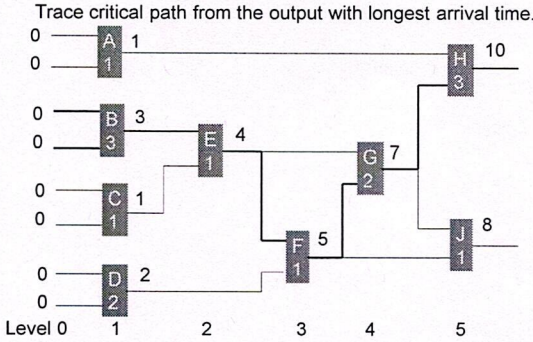
Example (Cont.)

Determine output arrival time when all input arrival times are known.

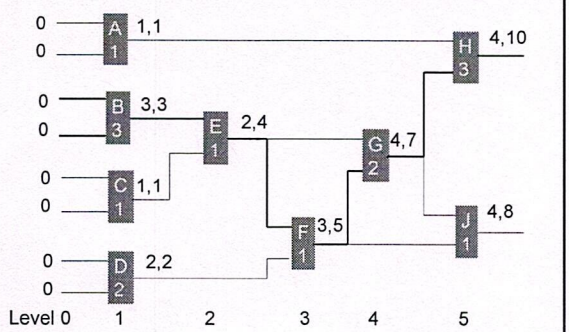


Example (Cont.)

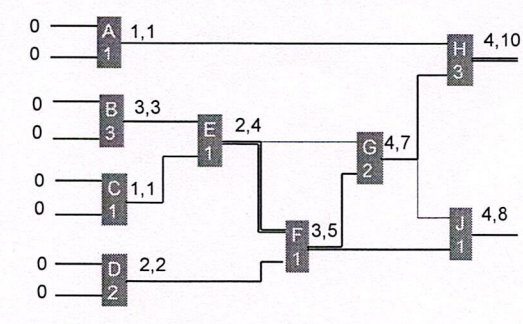
Trace critical path from the output with longest arrival time.



Finding Earliest and Longest Times



Shortest and Longest Paths



Characteristics of STA

- Linear time analysis, Complexity is O(n), n is number of gates and interconnects.
- Variations:
  - Find k longest paths:
    - S. Kundu, "An Incremental Algorithm for Identification of Longest (Shortest) Paths," *Integration, the VLSI Journal*, vol. 17, no. 1, pp. 25-35, August 1994.
  - Find worst-case delays from an input to all outputs.
  - Linear programming methods.

Algorithms for Directed Acyclic Graphs (DAG)

- Graph size: n = |V| + |E|, for |V| vertices and |E| edges.
- Levelization: O(n) (linear-time) algorithm finds the maximum (or minimum) depth.
- Path counting: $O(n^2)$ algorithm. Number of paths can be exponential in n.
- Finding all paths: Exponential-time algorithm.
- Shortest (or longest) path between two nodes:
  - Dijkstra's algorithm: $O(n^2)$
  - Bellman-Ford algorithm: $O(n^3)$

References

- Delay modeling, simulation and testing:
  - M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Springer, 2000.
- Analysis and Design:
  - G. De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994.
  - N. Maheshwari and S. S. Sapatnekar, *Timing Analysis and Optimization of Sequential Circuits*, Springer, 1999.
- PrimeTime (Static timing analysis tool):
  - H. Bhatnagar, *Advanced ASIC Chip Synthesis, Second Edition*, Springer, 2002